

**IN THE CLAIMS:**

Please add new claims as follows:

- 1-12 (Cancelled)
13. (Withdrawn) A method of manufacturing a semiconductor integrated circuit device including a memory cell constituted by a MISFET and a capacitor, comprising steps of:
- forming the MISFET on a semiconductor substrate;
- forming an insulating film on said MISFET;
- depositing a first shielding film on said insulating film;
- depositing, on an upper surface of said first shielding film,
- a first conductive film, a capacitive insulating film comprised of a high-dielectric-constant material, and a second conductive film; patterning said second conductive film and said capacitive insulating film exclusive of said first shielding film; and thereby forming, on said first
- shielding film, a capacitor constituted by a lower electrode comprised of said first conductive film, said capacitive insulating film, and an upper electrode comprised of said second conductive film; and
- forming a second shielding film covering sidewalls of said upper electrode and said capacitor and being comprised of an insulating film contacting with an upper surface of said first shielding film,
- wherein said capacitor is disposed on said MISFET through said insulating film,
- said capacitor is covered with said first and second shielding films,
- a plug is formed so that a conductive film is embedded into a first contact hole formed by removing said insulating film and said first shielding film on a source or drain region of said MISFET, said plug being connected to said lower electrode,
- a second contact hole is formed in said insulating film disposed on the other of the source or drain region of said MISFET, and
- the other of the source or drain region of said MISFET is connected through said second contact hole to a wiring formed on an upper portion of said insulating film.

14. (Withdrawn) The method of manufacturing a semiconductor integrated circuit device according to claim 13,  
wherein said first shielding film is formed so as to cover a forming region of said MISFET, and  
said second contact hole is formed in said first shielding film.
15. (Withdrawn) The method of manufacturing a semiconductor integrated circuit device according to claim 14,  
wherein said second shielding film is formed so as to cover a formation region of said MISFET, and  
said second contact hole is formed in said second shielding film.
16. (Withdrawn) The method of manufacturing a semiconductor integrated circuit device according to claim 14, wherein said first shielding film is comprised of an insulating film.
17. (Withdrawn) The method of manufacturing a semiconductor integrated circuit device according to claim 13, wherein said step of forming the insulating film includes a step of annealing in a hydrogen atmosphere.
18. (Withdrawn) A method of manufacturing a semiconductor integrated circuit device including a memory constituted by a MISFET and a capacitor, comprising steps of:  
forming a MISFET on a semiconductor device;  
forming an insulating film on said MISFET;  
depositing a first shielding film on said insulating film;  
depositing a first conductive film, a capacitive insulating film comprised of a ferroelectric material, and a second conductive film on said first shielding film; patterning said second conductive film and said capacitive insulating film exclusive of said first shielding film; and thereby forming, on said first shielding film, a capacitor constituted by a lower electrode comprised of said first conductive film, said capacitive insulating film, and an upper electrode comprised of the second conductive film; and

forming a second shielding film comprised of an insulating film so as to cover sidewalls of said upper electrode and said capacitor and contact with said first shielding film,

wherein said capacitor is disposed on said MISFET through said insulating film,

said capacitor is covered with said first and second shielding films,

said first shielding film is formed so as to cover a formation MISFET forming region,

a plug is formed so that a conductive film is embedded in a first contact hole formed by removing said insulating film and said first shielding film disposed on a source or drain region of said MISFET, said plug being connected to said lower electrode,

a second contact hole is formed in said insulating film disposed on the other of the source or drain region of said MISFET, and

the other of the source or drain region of said MISFET is connected to a wiring through said second contact hole.

19. (Withdrawn) The method of manufacturing a semiconductor integrated circuit device according to claim 18,

wherein said second shielding film is formed so as to cover the said MISFET forming region,

said second contact hole is formed in said second shielding film, and

said first shielding film is comprised of an insulating film.

20. (Withdrawn) The method of manufacturing a semiconductor integrated circuit device according to claim 18, wherein said wiring is formed on an upper portion of said insulating film.

21. (Previously Presented) A semiconductor integrated circuit device comprising:

(a) an information transfer MISFET including a gate insulating film formed over a semiconductor substrate, a gate electrode formed over the gate insulating film, and source and drain regions formed in the semiconductor substrate on both sides of said gate electrode;

(b) an insulating film formed over said information transfer MISFET;

(c) a capacitor including a lower electrode comprised of a first conductive film, a capacitive insulating film formed over said lower electrode and comprised of a high-dielectric or ferrodielectric material, and a lower electrode comprised of a second conductive film and electrically connected to one of said source and drain regions; and

(d) a first shielding film comprised of an insulating film formed under said lower electrode and a second shielding film comprised of an insulating film formed on said upper electrode,

wherein said capacitor is covered with said first and second shielding films,

said capacitor is formed over said source or drain region of said information transfer MISFET through said insulating film,

said first shielding film and second shielding film are formed over said source and drain regions of said information transfer MISFET, and

a plug is formed in a contact hole formed by removing said insulating film and said first shielding film located on another of said source and drain regions of said information transfer MISFET, with a conductive film being embedded in the plug, and is connected to said lower electrode.

22. (Previously Presented) The semiconductor integrated circuit device according to claim 21,

wherein said first shielding film is formed by a pattern larger than that of said lower electrode, and

said second shielding film is formed so as to cover an upper surface and a sidewall of said upper electrode, a sidewall of said capacitive insulating film, and a sidewall of said lower electrode by being connected to said first shielding film outside said lower electrode.

23. (Previously Presented) A semiconductor integrated circuit device comprising:

(a) an information transfer MISFET including a gate insulating film formed over a semiconductor substrate, a gate electrode formed over the gate insulating film, and source and drain regions formed in the semiconductor substrate on both sides of said gate electrode;

(b) an insulating film formed over said information transfer MISFET;

(c) a capacitor including a lower electrode comprised of a first conductive film

formed over said insulating film, a capacitive insulating film formed over said lower electrode and comprised of a high-dielectric or ferrodielectric material, and an upper electrode comprised of a second conductive film; and

(d) a shielding film formed so as to cover a sidewall of said lower electrode and an upper portion and a sidewall of said upper electrode,

wherein said shielding film includes a second shielding film formed by a pattern larger than that of said lower electrode and covering the upper portion and sidewall of said upper electrode, and a first shielding film formed under said second shielding film and formed so as to overlap with said second shielding film outside said lower electrode,

said first and second shielding films are each comprised of an insulating film,

said capacitor is formed over said source or drain region of said information transfer MISFET through said insulating film,

said first shielding film and said second shielding film are formed on said source and drain regions of said information transfer MISFET,

a plug is formed in a first contact hole formed by removing said insulating film and said second shielding film located on one of said source and drain regions of said information transfer MISFET, with a conductive film being embedded in the plug, and is connected to said lower electrode, and

a second contact hole is formed in said insulating film and said second shielding film located on another of said source and drain regions of said information transfer MISFET, and is connected to a wiring.

24. (Previously Presented) The semiconductor integrated circuit device according to claim 21,

wherein said second shielding film is formed by a pattern larger than that of said lower electrode, and

said first shielding film is formed so as to overlap with said second shielding film outside said lower electrode.

25. (Previously Presented) The semiconductor integrated circuit device according to claim 21,

wherein said first and second shielding films and said capacitive insulating film are insulating films each made of a lead compound, and

a lead composition ratio of each of said shielding films is set higher than that of said capacitive insulating film.

26. (Previously Presented) The semiconductor integrated circuit device according to claim 21, wherein said capacitive insulating film is a first PZT film ( $Pbx_1(Zry_1Tiz_1)O_3$ ), and  
said first and second shielding films are second PZT films ( $Pbx_2(Zry_2Tiz_2)O_3$ ) ( $X_2 > X_1$ ).
27. (Previously Presented) The semiconductor integrated circuit device according to claim 21,  
wherein an interlayer insulating film having barrier layers on said information transfer MISFET and capacitor is formed, and  
a wiring is formed on said interlayer insulating film.
28. (Previously Presented) The semiconductor integrated circuit device according to claim 27, wherein said barrier layer is made of a lead compound or is a PZT film, Al<sub>2</sub>O<sub>3</sub> film or amorphous film.
29. (Previously Presented) The semiconductor integrated circuit device according to claim 27, further comprising: a contact hole formed in said interlayer insulating film, wherein bottom and side portions of said contact hole are covered with a TiN film.
30. (Previously Presented) The semiconductor integrated circuit device according to claim 27, further comprising:  
a plurality of wirings including said wiring; and  
another interlayer insulating film having the same constitution as that of said interlayer insulating film formed between the wirings.
31. (Previously Presented) The semiconductor integrated circuit device according to claim 27, further comprising: a passivation film formed on an uppermost layer of said plurality of wirings, wherein said passivation film having a barrier layer.
32. (New) A semiconductor integrated circuit device having an information transfer

MISFET and a capacitor connected in series to said information transfer MISFET, said device comprising:

(a) said information transfer MISFET constituted by a gate insulating film formed on a semiconductor substrate, a gate electrode formed on an upper portion thereof, and source and drain regions formed in the semiconductor substrate located at both sides of said gate electrode;

(b) an insulating film formed on said information transfer MISFET;

(c) said capacitor constituted by a lower electrode composed of a first conductive layer, a capacitive insulating film formed on said lower electrode and made of a ferroelectric material, and an upper electrode formed on said capacitive insulating film and composed of a second conductive film; and

(d) a first shielding film formed under said lower electrode, and a second shielding film formed on said upper electrode,

wherein a memory cell is composed of said information transfer MISFET and said capacitor,

said memory cell forms a nonvolatile memory using a binary characteristic of a polarization state of said ferroelectric material,

said first shielding film and said second shielding film form shielding films for preventing entry of hydrogen into said capacitive insulating film,

said capacitor is covered with said first and second shielding films,

said second shielding film is formed so as to cover an upper portion and a sidewall of said upper electrode and a side surface of said capacitive insulating film, and a sidewall of said lower electrode is formed so as not to be covered with said capacitive insulating film and so as to be covered with said second shielding film,

said first shielding film is formed in a pattern larger than said lower electrode,

said capacitor is formed on said source or drain region of said information transfer MISFET via said insulating film,

a plug is formed by embedding a conductive film in a contact hole which is formed by removing said insulating film and said first shielding film on said source or drain region of said information transfer MISFET, and

said plug is connected to said lower electrode on said source or drain region of said information transfer MISFET.

33. (New) The semiconductor integrated circuit device according to claim 32, wherein

said second shielding film is connected to said first shielding film on the outer side of said lower electrode and is formed so as to cover an upper surface and a sidewall of said upper electrode, a sidewall of said capacitive insulating film, and a sidewall of said lower electrode.

34. (New) A semiconductor integrated circuit device having an information transfer MISFET and a capacitor connected in series to said information transfer MISFET, said device comprising:

(a) said information transfer MISFET constituted by a gate insulating film formed on a semiconductor substrate, a gate electrode formed on an upper portion thereof, and source and drain regions formed in the semiconductor substrate located at both sides of said gate electrode;

(b) an insulating film formed on said information transfer MISFET;

(c) said capacitor constituted by a lower electrode formed on said insulating film and composed of a first conductive layer, a capacitive insulating film formed on said lower electrode and made of a ferroelectric material, and an upper electrode formed on said capacitive insulating film and composed of a second conductive film; and

(d) a shielding film formed so as to cover a sidewall of said lower electrode, an upper portion and a sidewall of said upper electrode,

wherein a memory cell is composed of said information transfer MISFET and said capacitor,

said memory cell forms a nonvolatile memory using a binary characteristic of a polarization state of said ferroelectric material,

said shielding film is formed in a pattern larger than said lower electrode and includes a second shielding film covering an upper portion and a sidewall of said upper electrode and a first shielding film formed below said second shielding film so as to overlap said second shielding film on the outer side of said lower electrode,

said second shielding film is formed so as to cover an upper portion and a sidewall of said upper electrode and a side surface of said capacitive insulating film, and a sidewall of said lower electrode is formed so as not to be covered with said capacitive insulating film and so as to be covered with said second shielding film,

said first and second shielding films are composed of insulating films and form shielding films for preventing entry of hydrogen into said capacitive insulating

film,

    said capacitor is formed on said source or drain region of said information transfer MISFET via said insulating film,

    said first and second shielding films are formed on said source and drain regions of said information transfer MISFET,

    a plug is formed by embedding a conductive film in a first contact hole which is formed by removing said insulating film and said second shielding film on one of said source and drain regions of said information transfer MISFET,

    said plug is connected to said lower electrode on said source or drain region of said information transfer MISFET, and

    a second contact hole is formed in said insulating film and said second shielding film on the other of said source and drain regions of said information transfer MISFET.

35. (New) The semiconductor integrated circuit device according to claim 34, wherein  
    said second shielding film is formed in a pattern larger than said lower electrode, and  
        said first shielding film is formed so as to overlap said second shielding film  
        on the outer side of said lower electrode.